CHAPTER 2

DESCRIPTION

GENERAL DESCRIPTION

The Model RS-690 is a high-speed (250 MHz), highly-adaptable Digital Word Generator capable of generating time variant digital output waveforms. It features menu-structured software for programming the available formats and control operations. Programming is accomplished via the front panel keyboard or remotely via RS-232 or IEEE 488 interfaces (standard). Menus and data are displayed on the integral front panel CRT or via an external composite video monitor.

The RS-690 is comprised of a CRT, two power supplies, a floppy disk drive (optional), and four main circuit cards: the Central Processing Unit (CPU) card; Period Clock Generator (PCG) card; and, depending upon configuration, one or two High Speed Memory (HSM) cards. See Operational Description section for a detailed description of these components. In addition, the RS-690 can be variously configured with three types of data and clock pods. See Options section for a detailed description of the pods.

The CPU card controls all interfacing for test measurement set-up through the front panel CRT and keyboard, or the remote interfaces.

Controls and indicators are mounted on the front panel of the enclosure. Output pod connectors are located on the rear panel. Front panel controls and indicators are shown in figure 2-1 and described in table 2-1. Rear panel connectors are shown in figure 2-2 and described in table 2-2.

Remote control and programming of the unit by a host device is accomplished through the IEEE 488 and RS-232C ports on the rear panel of the unit. Any host device capable of generating standard ASCII command characters may be used.

The Period Clock Generator (PCG) card contains the high speed clock circuitry that drives the High Speed Memory (HSM) output cards. The PCG circuit card assembly is comprised of a 500 MHz oscillator and two custom gate arrays: the programmable clock and address array, and; the table sequence array.

The High Speed Memory (HSM) card(s) contains high-speed memory for data word output. Output from memory is controlled by gate arrays and output through 16-channel connectors.

The programmable clock and address gate array produces the programmable output clock, programmable output sync signals, and output RAM memory addresses. This array has the capability of changing periods on the fly, with no signal discontinuity, and determines the final output shift mode (number of output words per internal memory word). This gate array also implements the Timing Simulation mode, in which a state is output and held for a programmed interval.

The table sequence array contains the table sequencer logic for controlling the memory address presetting, which provides for three-level table sequencing functions. For a thorough discussion of table sequencing, see the SEQUENCE section of Chapter Three, Local Operation.

Several external inputs are also brought into this card. For user-specific clock frequencies, an external clock signal can be provided, and either the rising or falling edge can be selected for data output. An external start trigger and a gate interrupt signal also help to control the output pattern.

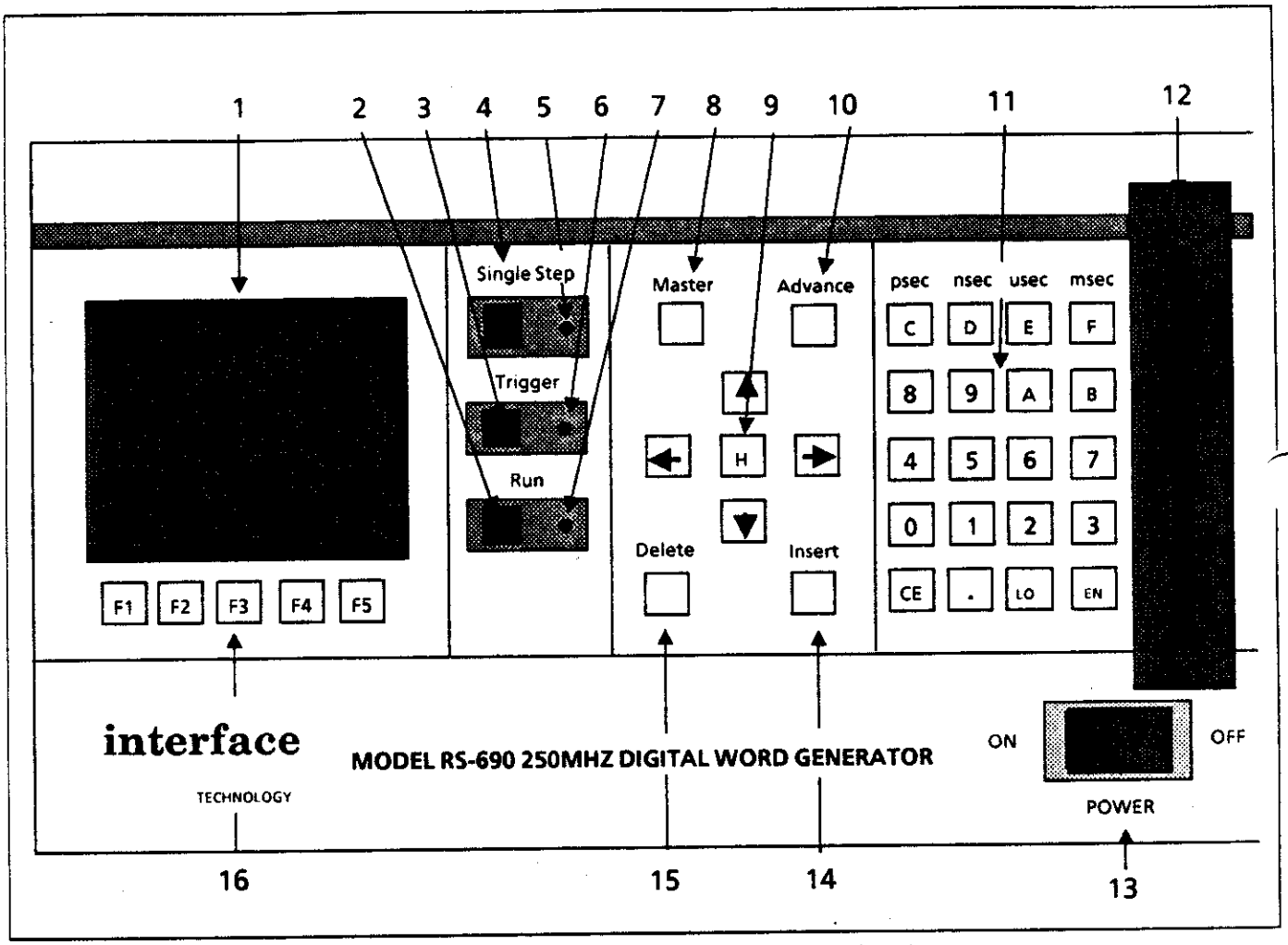

Figure 2-1. RS-690 Front Panel Controls and Indicators

The RS-690 generates word sequences through the manipulation of memory addresses, which are then converted to a digital waveform for output. Unique RAM contents may be addressed, with different data being output for each clock cycle. Digital control of delay and amplitude functions provides the capability for precise control over waveform amplitude and edge placement. Exact values may be directly programmed and stored on disk, without the need to fine tune settings for every test.

The RS-690 can be configured with a maximum of 128 channels with the optional second High Speed Memory (HSM) card installed.

Mass storage in the form of an optional 5-1/4 floppy disk drive is also available. Data is stored on double-sided, double-density (9 sector) disks formatted for MS-DOS (2.0 or newer). The set-up menu parameters and pattern data are stored in ASCII, making it easy to edit files off-line or to write a simple data format translator. The use of a mass storage device provides the advantage of saving and reusing particular test set ups.

Pattern data is output to the Unit Under Test (UUT) via data pods. TTL, ECL, and Variable Current pods are available as options. These pods may be combined in any configuration and number up to the maximum number of connectors available (four with the standard HSM card, eight with the optional second card, plus one clock connector), providing greater test configuration flexibility. However, pods of different logic families produce different delays which may affect critical skew alignment between data channels. See Appendix C for detailed specifications on pod delay characteristics.

Pre-Set up Considerations

The RS-690 offers many tradeoffs between memory depth, number of data output channels, and the maximum data rate for those channels. The degree of flexibility afforded the user by the design of the RS-690 also makes it necessary to carefully consider beforehand the optimal configuration for the particular application under consideration.

There are primarily four interrelated parameters which must be considered when designing a test: operating mode; number of channels per connector; speed; and memory data depth.

Table 2-1. RS-690 Front Panel Controls and Indicators

INDEX NO	NOMENCLATURE	FUNCTION
1	CRT	Primary display for all menus, prompts, and error information.
2	RUN key	Enables the RS-690 to run selected program or to halt the execution of the program.
3	TRIGGER key	Provides manual triggering of the RS-690.
4	SINGLE STEP key	Outputs next data word during single step operation.
5	SINGLE STEP LED	When illuminated, indicates that Single Step operation is enabled.
6	TRIGGER LED	When illuminated, indicates that the RS-690 is waiting for the application of a trigger.
7	RUN LED	When illuminated, indicates that the RS-690 is in the run mode.
8	MASTER key	When pressed, causes the MASTER menu to be displayed on the unit CRT.
9	Cursor Control keys	Four arrow keys used to manually position the cursor to the next available option or data entry location. The HOME key will return the cursor to the specified HOME location for each displayed menu.
10	ADVANCE key	The result of pressing the ADVANCE key depends upon the cursor position at the time the key is pressed. Pressing the ADVANCE key with the cursor on the MODE, #CHAN/CONN, or SETUP fields cycles the software through the SETUP submenus. Pressing the ADVANCE key with the cursor on any of the CONTROL fields cycles the software to the corresponding menu, then back to the MASTER menu.
11	Hexadecimal key pad	Contains three function keys, (ENTR, CE, and LOC) and sixteen data entry keys (0-9, A-F) of which four have dual functions (pSEC, nSEC, uSEC, mSEC). Units of time are loaded using the C(pSEC), D(nSEC), E(uSEC), or F(mSEC) keys. The CE key is used to clear an invalid or erroneous entry.

Table 2-1. RS-690 Front Panel Controls and Indicators (Continued)

INDEX NO.	NOMENCLATURE	FUNCTION
	Hexadecimal Key Pad (Continued)	Pressing the ENTR key signifies the completion of a particular keyboard entry, and causes the cursor to advance to the next valid data entry field. Data entries in the DATA display do not require the use of the ENTR key. Pressing the LOC key returns the unit to local operation mode, enabling the front panel controls. When pressed in **LOCAL** mode, the LOC key acts as a system reset key.
12	Disk Drive	Units equipped with the Disk Drive assembly have 360 Kbytes of storage for menu configurations and test data files.
13	POWER switch	Controls the application of power to the RS-690.
14	INSERT key	Used to insert tables in the TABLE menu and in the SEQUENCE menu.
15	DELETE key	Used to delete tables in the TABLE menu and in the SEQUENCE menu.
16	Function keys	Five pushbuttons (F1, F2, F3, F4 and F5) that correspond to operator prompts displayed on the lower portion of the CRT.

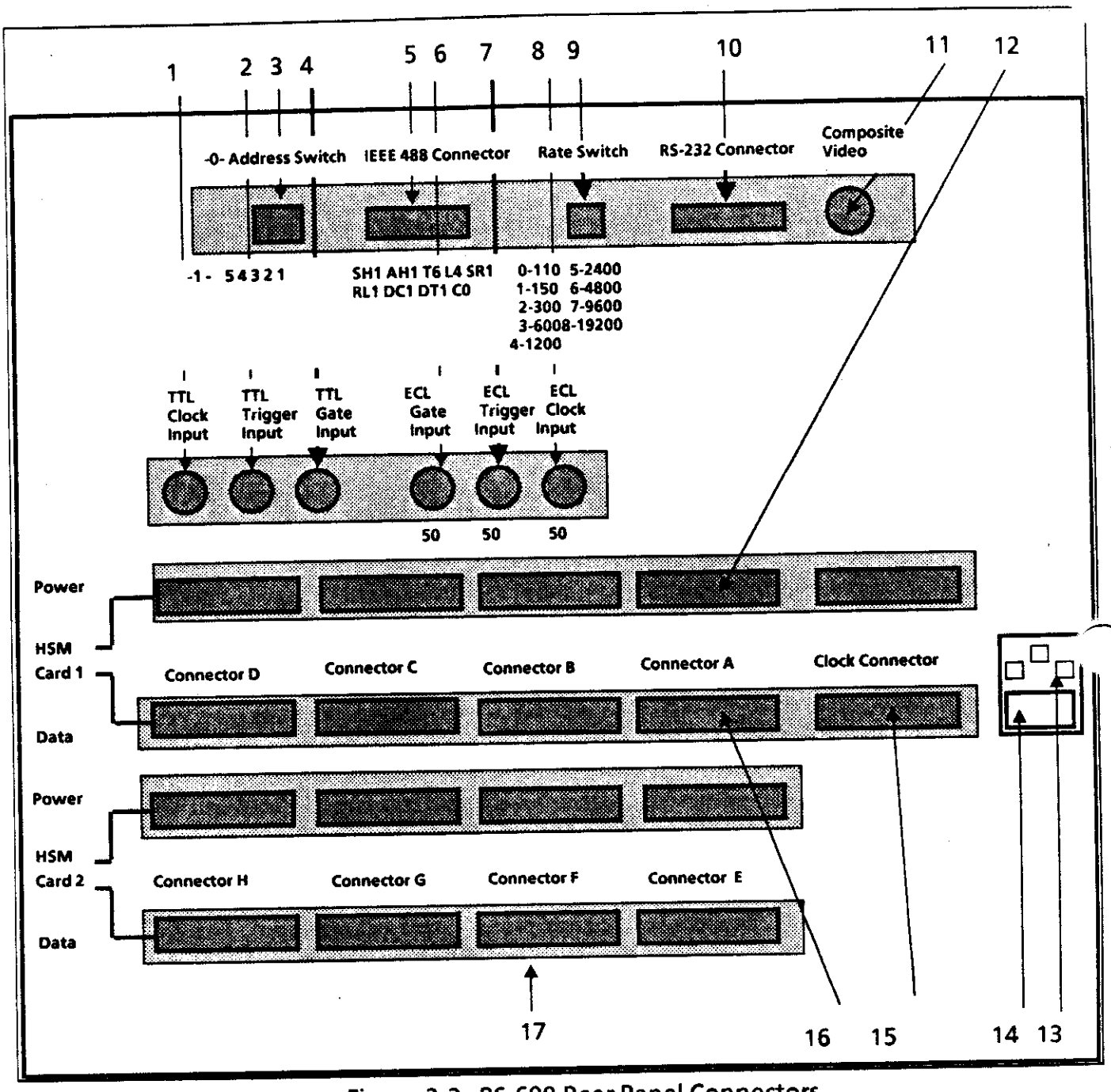

Figure 2-2. RS-690 Rear Panel Connectors

Table 2-2. RS-690 Rear Panel Connectors

INDEX NO	NOMENCLATURE	FUNCTION
1	TTL Clock Input	Allows use of a TTL level external clock.
2	TTL Trigger Input	Allows use of a TTL level external trigger.
3	Address Switch	Selects IEEE remote control address.
4	TTL Gate Input	Inhibits clock when pulse is active.
5	IEEE 488 Connector	Provides the interface between RS-690 and a remote IEEE 488 controller.
6	ECL Gate Input	Inhibits clock when pulse is active. Standard input is terminated 50 ohms to -2V.
7	ECL Trigger Input	Allows use of a ECL level external trigger. Standard input is terminated 50 ohms to -2V.
8	ECL Clock Input	Allows use of a ECL level external clock. Standard input is terminated 50 ohms to -2V.
9	Rate Switch	Selects baud rate for RS-232C remote control interface.
10	RS-232 Connector	Provides the interface between RS-690 and a remote controller.
11	Composite Video	Provides the interface between RS-690 and a remote composite video monitor.
12	Power	Provides power to the pods.
13	AC Power Receptacle	Provides for connection of RS-690 unit to primary power source.
14	Fuse Holder	Container for 10A fuse. For 220V option, fuse is rated at 5A.
15	Clock Connector	Provides interface between the RS-690 and the clock pod.
16	Connectors A thru D	Resident on High Speed Memory card 1, each connector provides 16 channels of data output.
17	Connectors E thru H	Resident on High Speed Memory card 2, (optional), each connector provides 16 channels of data output.

Operational Mode

The RS-690 provides two modes of operation; Word Generator and Timing Simulator. The Word Generator mode provides a synchronous, steady-state clock rate, offering the greatest number of channel and memory depth options. The Timing Simulator mode provides the capability of programming variable state periods, rather than relying upon a fixed clock period for outputting each individual bit. This results in a savings of programming time

and memory space. For example, to program a 16*ns* high state followed by a 1*us* low state would require only two data words.

The Word Generator mode best fits applications which require synchronously clocked data, or data that is to be held for a regular interval. For every transition of the period clock, one data memory word will be generated. In this mode, the RS-690 can be programmed to output up to 128 channels of data, in which the operator has specified the clock period and sequence program. Output data may be displayed in hexadecimal, octal, or binary format.

The Timing Simulator mode provides a "shorthand" method of programming which best fits applications that require waveforms characterized by few state changes occurring over relatively long time intervals. When using Timing Simulation, the data state and its duration are specified. With this capability, short (4*ns*) pulses and long steady state waveforms can be created without using large amounts of memory.

Number of Channels

Output channels are arranged in groups of 16 channels per connector. A maximum of two High Speed Memory (HSM) cards can be used. Each memory card has a total of 64 channels, for a total of 128 channels possible. The maximum output frequency of programmed data is 250 MHz.

Speed and Data Depth

The maximum data output speed and maximum memory data depth are not directly programmed, but are determined by choosing the number of channels per connector. Table 2-3 provides a description of channel count, memory depth, and minimum pulse widths for the Word Generator and Timing Simulator modes.

Table 2-3. Configuration Options

Mode	#Chan/Conn	Max. Memory Depth	Min. Pulse Width
WG	16	1k	16ns
WG	8	2k	8ns
WG	4	4k	4ns
WG	2	8k	4ns
WG	1	16k	4ns
TS	16	1k	16ns
TS	8	1k	8ns
TS	4	1k	4ns

By using a variable output register, the number of data channels can be programmed, which allows multiple words to be output per each 16 bit internal memory word. The memory depth, or number of bits per data word is also determined by the number of channels per connector chosen.

TERMINOLOGY

Because both data rate and clock rate are defined in terms of frequency (MHz), misconceptions may arise when speaking in terms of data throughput versus clocking frequency. it is important to clarify the differences between clock and data waveforms.

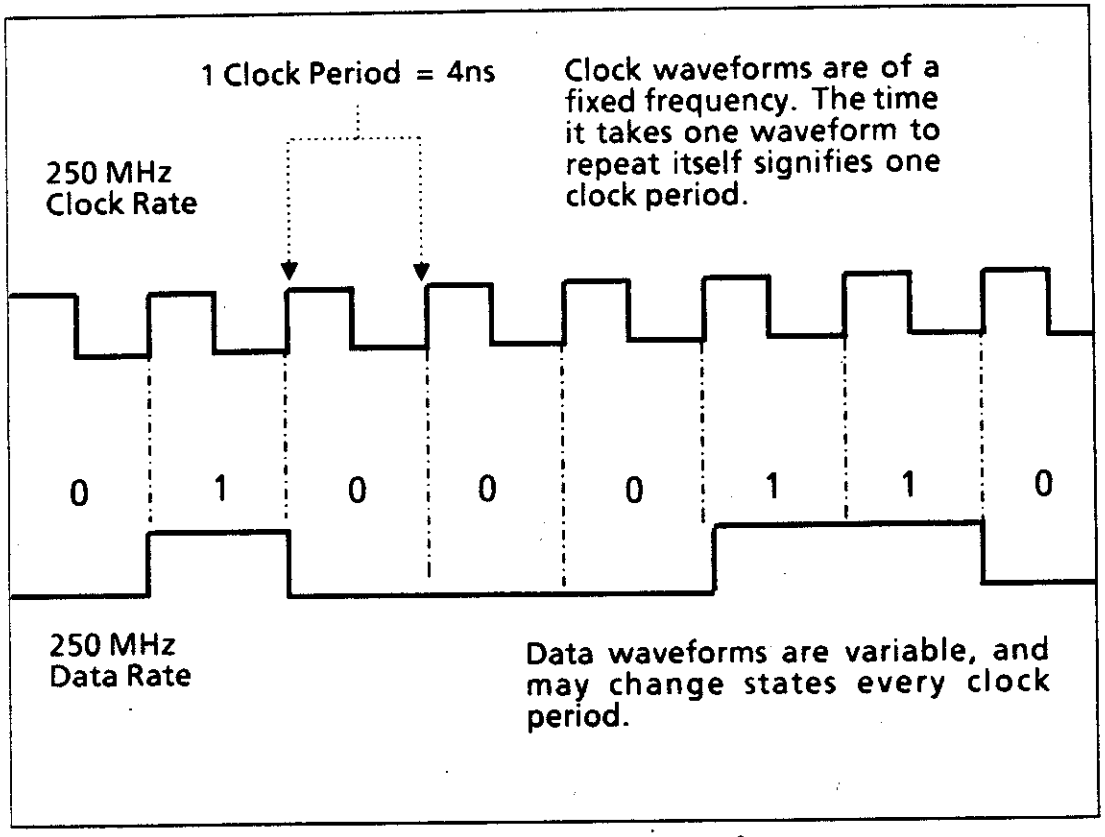

Figure 2-3 .Clock vs. Data Waveforms.

As this example shows, at the RS-690's maximum data rate of 250 MHz, the data is output every 4ns. Since the data in this example is nonrepetitive, it cannot be literally specified in terms of frequency. What is meant when speaking of a 250 MHz data rate is the RS-690's ability to clock out a data pulse every 4 ns. Another, and perhaps more accurate way of expressing data output in this case would be in terms of Mbits per second. The RS-690 can output one bit every 4ns, which is equivalent to 250Mbits/second ($1 \div 4x10^{-9} = 250 \times 10^{6}$).

Also, note that if a data channel is used to derive a clock, the maximum clock frequency would be 125 MHz.

OPERATIONAL DESCRIPTION

The RS-690 is designed to give the user maximum control and flexibility over the major parameters involved in generating waveforms for digital testing. This is possible because of the RS-690's software control over the output configuration, which includes the ability to choose tradeoffs between memory depth, number of data output channels, and the maximum data rate for those channels. The degree of flexibility afforded the user by the design of the RS-690 makes it necessary to take into account these tradeoffs when selecting the optimal configuration for the desired application.

The RS-690 uses an output shift register to enable the operator to indirectly control maximum data output rate and memory depth by setting the number of data output channels per connector to be used. The desired maximum data rate determines the output shift parameter, which affects the actual #chan/conn pattern and memory depth available. Data is stored in RAM in 16-bit words, which may be split into either eight, four, two, or one bit words by specifying the number of channels per connector. The data is then software shuffled to be output on the first sixteen, eight, four, two or one pin of the connector, depending upon the configuration. (Note: output speed depends upon period programmed.)

The following examples (figures 2-4 and 2-5) illustrate how the RS-690 accommodates a wide variety of test configurations.

If the test is configured for 4 channels per connector, the 16-bit data is divideo among the four channels, resulting in four, 4-bit data words. Although an internal 16-bit data word is being loaded into the shift/skew array at 62.5 MHz, the final 4-bit output words are being clocked out at 250 MHz.

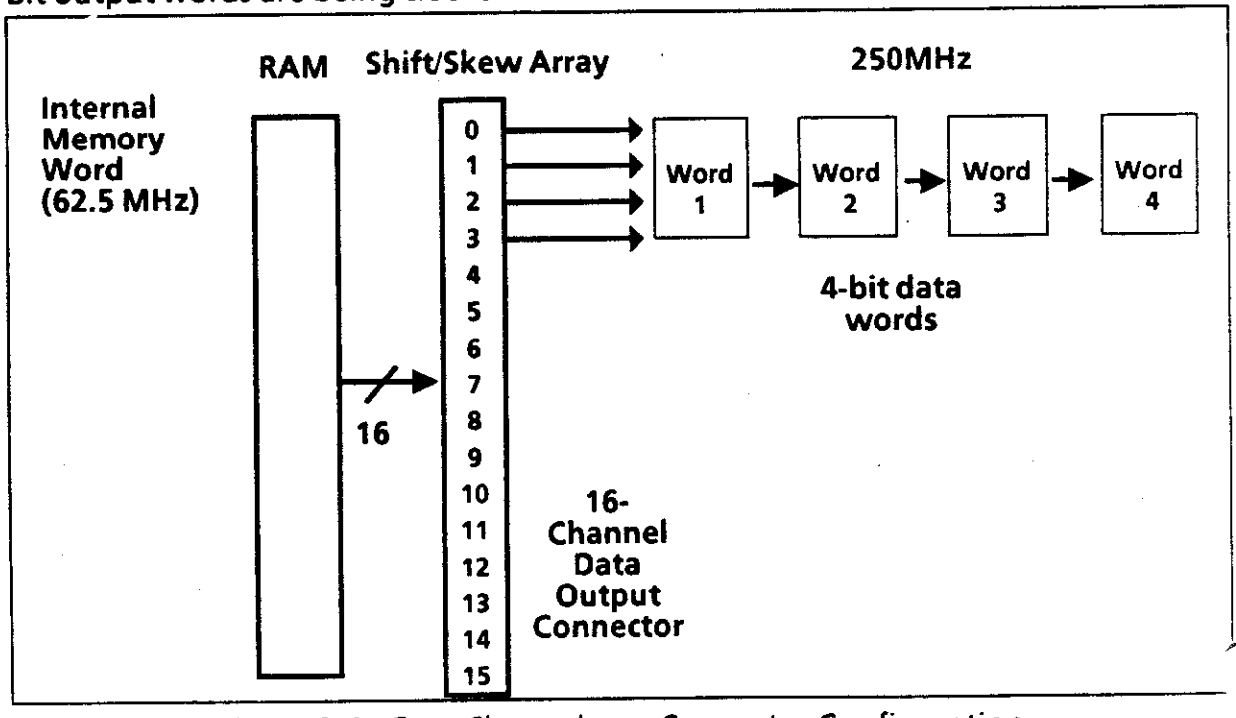

Figure 2-4. Four Channels per Connector Configuration

If the test is configured for 8 channels per connector, the 16-bit data is divided into 8-bit data, resulting in a maximum data output rate of 125 MHz, as illustrated below:

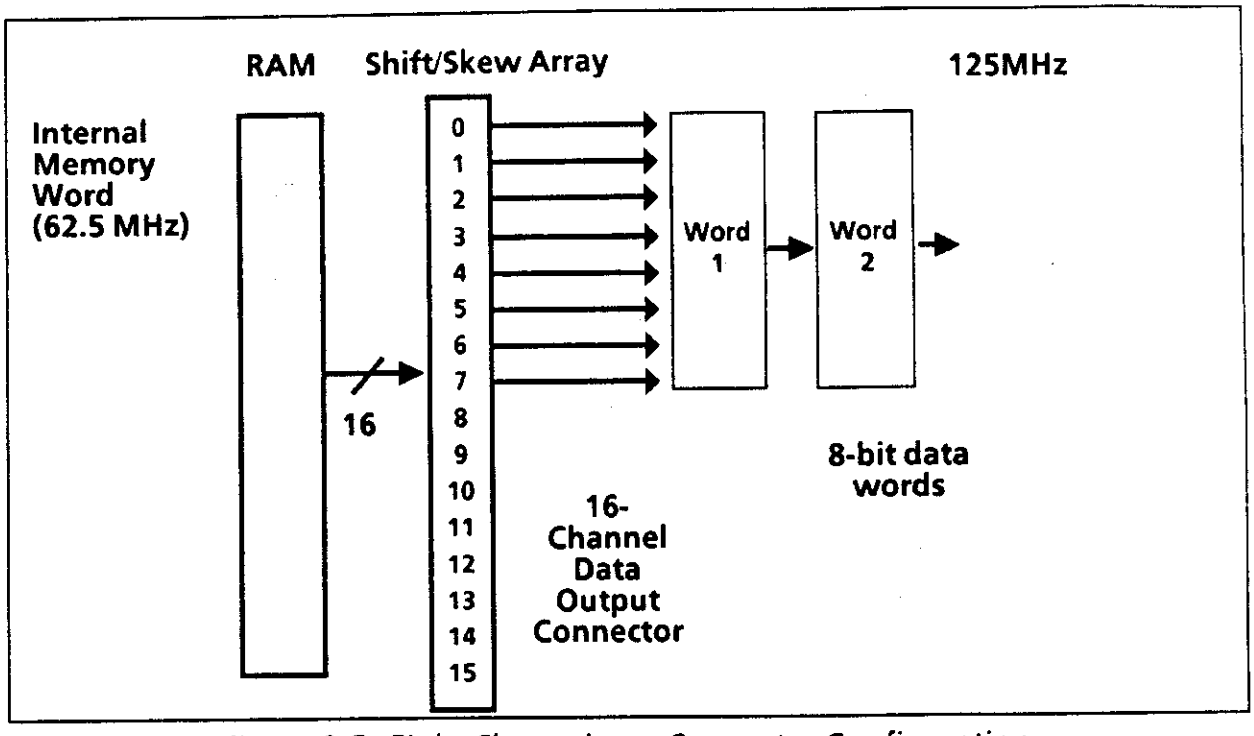

Figure 2-5. Eight Channels per Connector Configuration

FUNCTIONAL DESCRIPTION

CPU Card

The CPU circuit card is the main controlling card for all functions provided by the RS-690 Digital Word Generator. The card contains the components required to interface the unit with the internal CRT, the floppy disk drive (optional) and the remote control interfaces. The CPU also provides video to both the internal CRT and to the rear panel external video connector for use by an external display.

The CPU is based on the 6809E microprocessor. It uses up to 128K bytes of EPROM and up to 16K bytes of RAM, and contains the operational software for the unit. The 6809E is the main controller for the entire system, interfacing with the other installed cards to provide command and control data during set up and operation.

The CPU card microprocessor controls a bus connector which provides a common interface between the CPU, HSM and PCG cards. Through this interface, the microprocessor can read and write data to and from the PCG clock and sequence gate arrays, as well as the HSM. In addition, the PCG card can address the HSM through another high speed bus connector.

The CRT is controlled from the CPU card by the CRT Display Controller, providing the integral CRT with menu and data display information. The CRT controller provides data to the 46 character by 22 line CRT for information display, and accesses 2K x 16 bits of video RAM. The CRT controller is

programmed to provide inverse video, underline, blinking cursor, and high resolution video. The CRT controller also controls the video information that is routed to the external video connector mounted on the unit rear panel for use with an external video monitor.

The IEEE 488 and RS-232 interfaces on the CPU card are connected to the IEEE 488 and RS-232 ports, respectively, mounted on the rear panel.

The CPU card also contains the floppy disk controller for the 5¼ inch floppy disk drive assembly (optional), the front panel keyboard decoder and LED drivers, and the bus interface to control the other circuit cards.

HSM Card The High Speed Memory (HSM) circuit card contains a microprocessor interface which controls the data and control line interface between the microprocessor data bus and the HSM circuit card. The HSM card(s) receives commands and data from the CPU and PCG cards via the data and address buses during operation, and provides the interface between the unit under test (UUT) and the RS-690. The HSM card memory holds data to be output during the performance of a test program.

The High Speed Memory (HSM) card(s) contains high-speed memory in four 16-bit X 1Kbyte-deep banks. Data output from each of these memory banks is controlled by a shift and skew gate array which groups data into a preprogrammed number of bits per output word. Each array outputs data to a sixteen-channel output connector. The number of channels that data are output through is also software controlled.

PCG Card The PCG circuit card contains the clock selection logic to allow the unit to operate from the selected clock source . The selected clock source is controlled by the clock drivers mounted on the PCG card to buffer and gate the clocks for distribution throughout the PCG card and to the High Speed Memory card(s) within the unit. Also contained within the clock selection logic is the trigger logic which allows selection of using a variety of triggers to start the unit.

POWER DISTRIBUTION

AC input power enters the RS-690 through the rear panel mounted AC input connector and is routed to the solid state relay (SSR) through the main power fuse (F1) mounted on the inside of the rear panel. The SSR provides protection against power surges and transient line voltages for the power supply installed in the RS-690. From the SSR, the AC power is routed to the front panel switch. See figure 2-7 for RS-690 intercabling. See figure 2-8 for RS-690 DC power distribution, and figure 2-9 for AC power distribution.

When the main power switch is placed to the ON position, AC power is applied to the fans to provide cooling during operation and to the internal power supply, where line voltage is converted to +15, -15, +12, -12, +5, -4.5, and -2 VDC power levels.

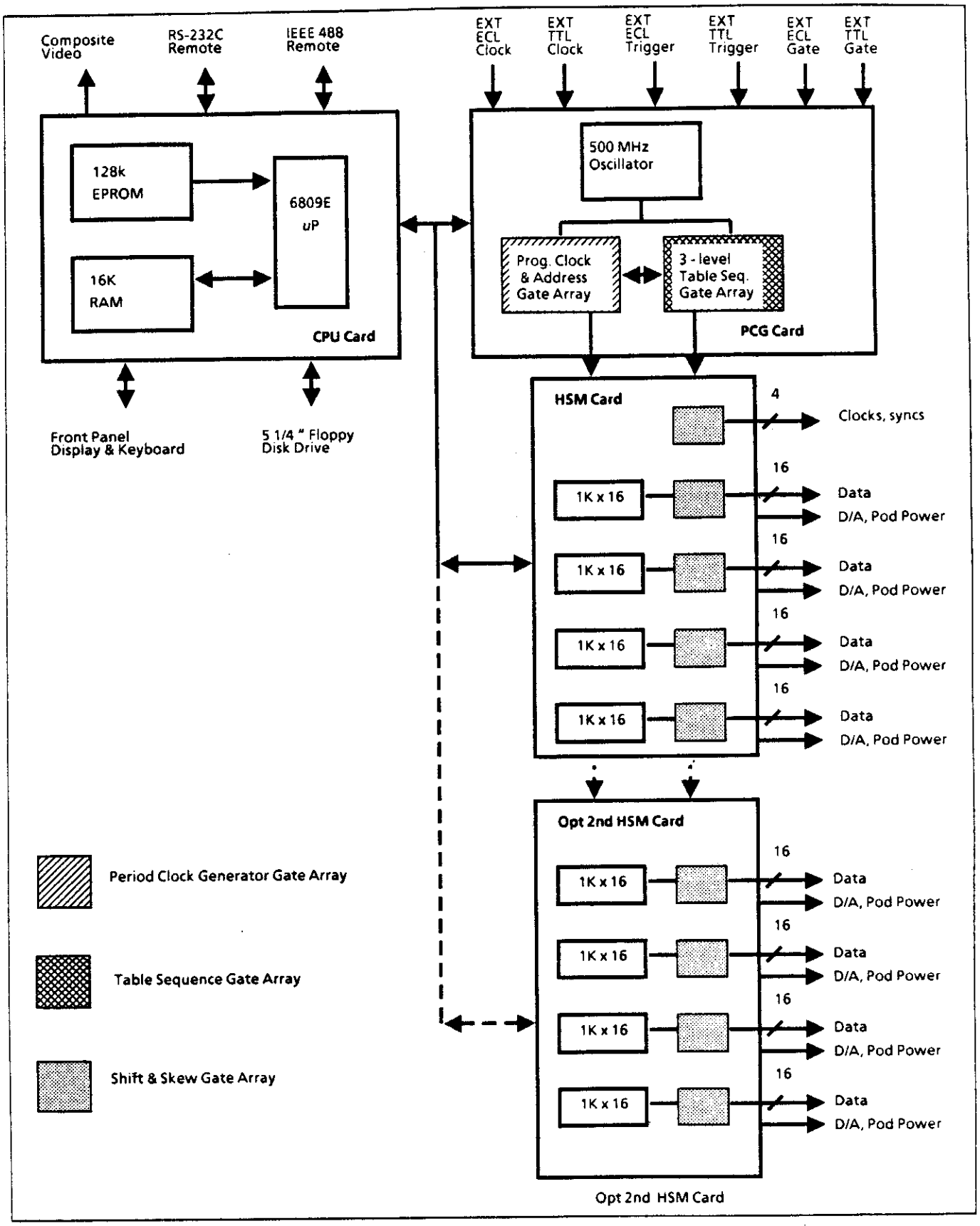

Figure 2-6. RS-690 Functional Block Diagram

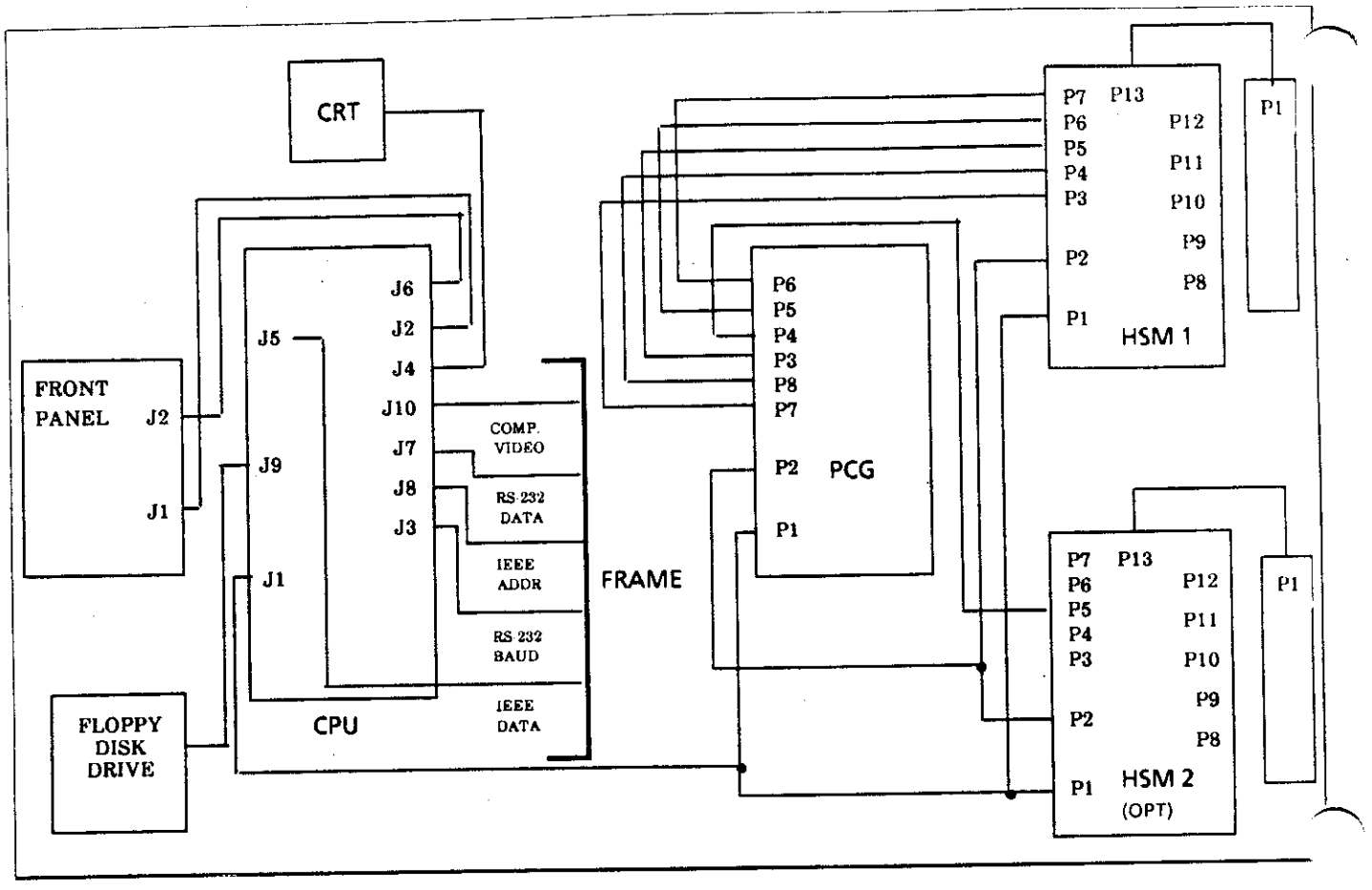

Figure 2-7. RS-690 Intercabling Diagram

The power supply DC outputs are routed to the appropriate components within the RS-690 mainframe, and the interconnecting wiring is color coded as to the voltage of each line.

The power supply provides operating power to the Central Processing Unit (CPU), Period Clock Generator (PCG), and High Speed Memory (HSM) circuit cards, the CRT, the front panel LED indicators, the Pod Power connector on the rear panel, and the Disk Drive assembly.

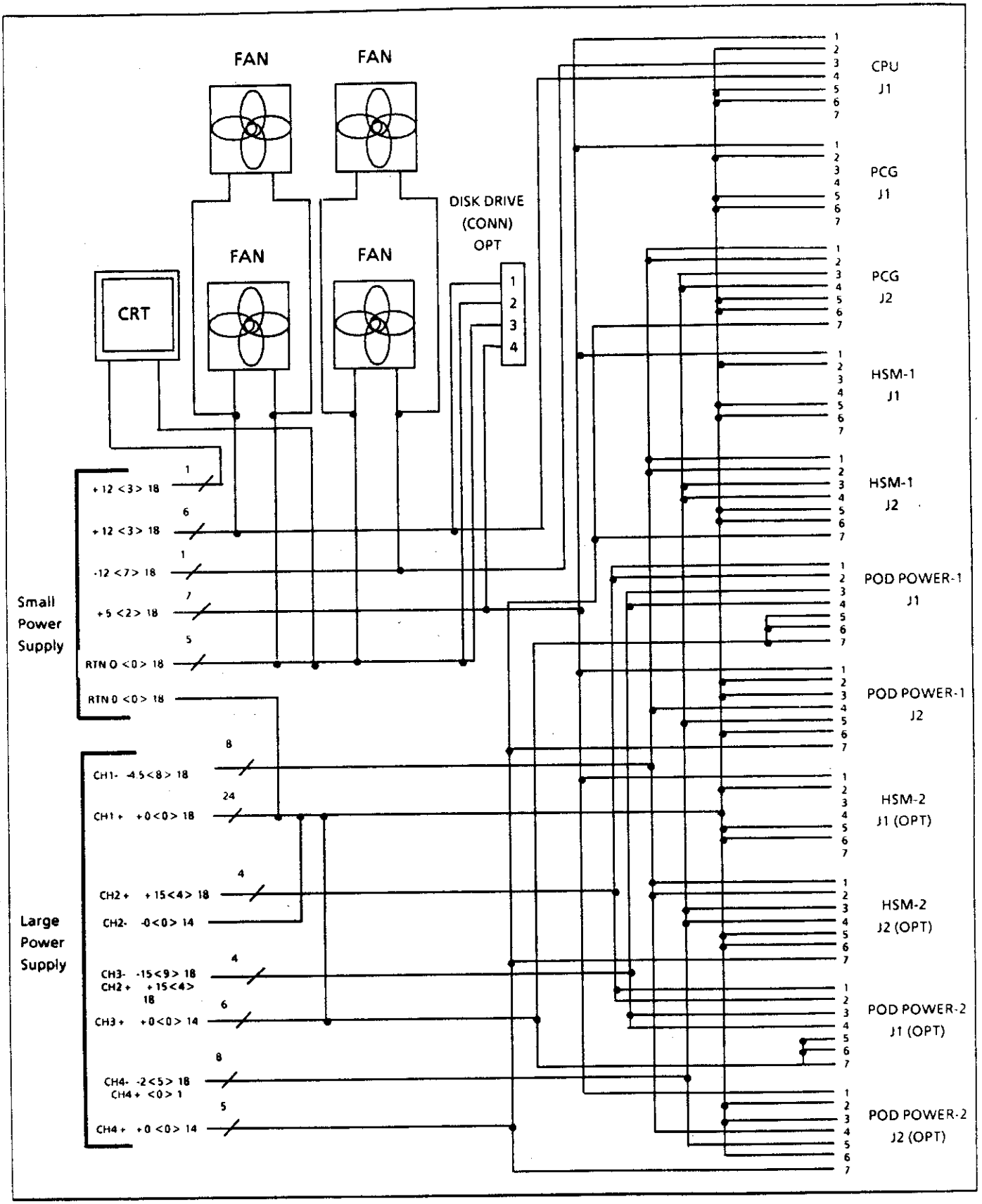

Figure 2-8. RS-690 DC Power Distribution

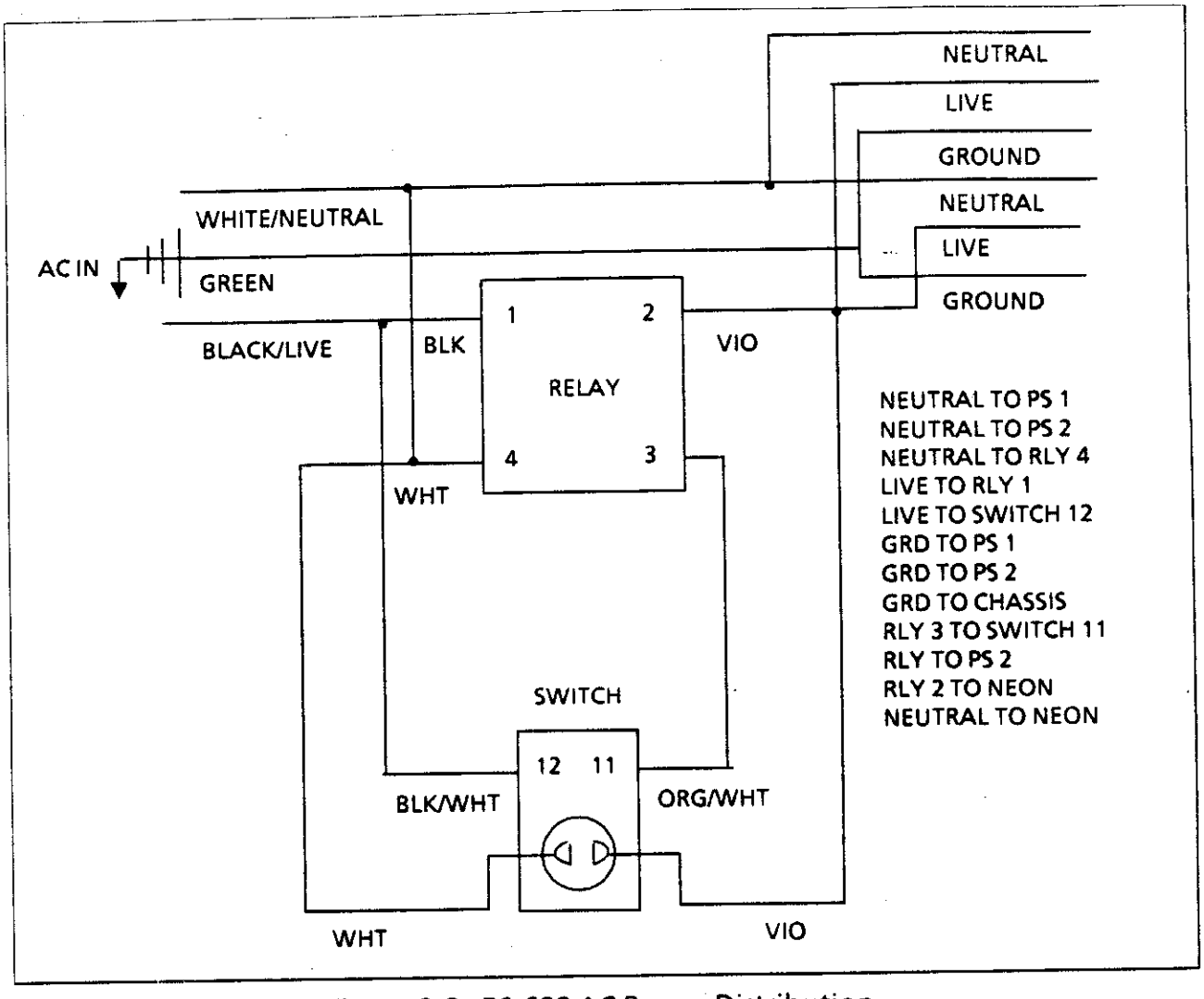

Figure 2-9. RS-690 AC Power Distribution

OPTIONS

The following paragraphs provide a brief description of options available for the RS-690 Digital Word Generator. Refer to Chapter 3 for detailed operational information. NOTE: The unit is factory calbrated for skew accuracy for a specific configuration. If this configuration is changed in the field by adding, subtracting, or moving pods to different connectors, specifications are no longer valid.

Additional High-Speed Memory (HSM) Card (Option 690-001).

A second HSM card can be installed in the RS-690, and is identical to the first one, but does not output clock signals. This card doubles the number of output data channels available.

Floppy Disk (Option 690-002).

A 5-1/4" floppy disk drive can be mounted in the unit, providing mass data storage capabilities. The disk drive's IBM compatibility (DOS 2.0 or newer) allows for

reading and organization of files on any PC. The RS-690 can access up to 64 files from the root directory of a disk.

125 MHz TTL Output Data Pod (Option 690-003)

The TTL data pod generates a TTL logic environment between the RS-690 and the UUT. Each unit provides sixteen separate, single-ended TTL-level data output channels. TTL levels are generated by ECL to TTL translators of the 100125 family. NOTE: See Appendix A for detailed pod termination information.

250 MHz ECL Output Data Pod (Option 690-004).

The ECL data pod generates a 100k ECL level environment between the RS-690 and the UUT. Each unit provides sixteen separate, ECL-level data output channels. NOTE: See Appendix A for detailed pod termination information.

250 MHz Variable Current Output Data Pod (Option 690-005)

The variable current data pod allows the user to program high and low levels for data output and vary it anywhere within a ±2.5V range in 10mV increments, with a 2.5V maximum amplitude, into a 50-ohm load. The pod provides up to four separate output channels. The amplitude levels for the four channels are collectively controlled. NOTE: See Appendix A for detailed pod termination information.

62.5 MHz TTL Output Clock Pod (Option 690-006)

The TTL output clock pod provides an external TTL level clock to the UUT. The unit provides four separate, single-ended TTL-level clock output channels: internally programmable sync; major loop sync; period clock, and; access to the RS-690's internal system clock. NOTE: See Appendix A for detailed pod termination information.

250 MHz ECL Output Clock Pod (Option 690-007)

The ECL output clock pod provides an external 100k ECL level clock to the UUT. The unit provides four separate, ECL-level clock output channels: internally programmable sync; major loop sync; period clock; and access to the RS-690's internal 250 MHz clock. NOTE: See Appendix A for detailed pod termination information.

250 MHz Variable Current Output Clock Pod (Option 690-008)

The clock pod provides an external variable voltage clock to the UUT. The unit provides four separately controllable clock output channels: internally programmable sync; loop sync; period clock; and access to the RS-690's internal system clock. The output levels for the four channels are collectively controlled NOTE: See Appendix A for detailed pod termination information.

220VAC Conversion (Option 690-009)

Converts standard 110 VAC unit to 220 VAC operation.